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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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TROP PRUNER & HU, PC
8554 KATY FREEWAY
SUITE 100
HOUSTON, TX 77024

EXAMINER	
AMINI, JAVID A	
ART UNIT	**PAPER NUMBER**
2672	

DATE MAILED: 10/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/584,604	ROSENBERG, SCOTT A.
	Examiner	Art Unit
	Javid A Amini	2672

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☒ Claim(s) *1-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-25 rejected under 35 U.S.C. 102(b) as being anticipated by Patrick et al. US patent 5,706,483 published date of Jan. 6, 1998, and filling date of Dec. 13, 1994.

1. Claim 1,

Patrick et al., hereinafter Patrick, shows a method comprising "writing pixel data to a first memory location", see disclosure in (Col. 6, lines 15-35) the following example that provides, what is involved in the block transfer of bytes from a source to a destination in memory. Patrick also shows "performing a first pixel transformation at said first memory location"; see Fig. 3 is a diagram showing an 8(1, 16, 32) bit per pixel bitmap at a source (a "source bitmap or first memory location") for transfer to an 8 bpp bitmap at a destination (a "destination bitmap or second memory location"). Patrick shows a complete illustration of "generating a memory address for a second memory location", see Fig. 3, that the source bitmap 60 is located at memory addresses 0-499 (decimal) and the destination bitmap 62 is located at memory addresses 900-1399. A data block 61 for transfer is contained within a rectangle 60a in source bitmap 60 and consists of 15 bytes on each of 5 consecutive scan lines at the memory addresses given in the figure. Patrick demonstrates the transformation of data from first location to second location "writing said transformed pixel data from said first memory location to said second memory location", see Figs. 4-5, data block 61 is to be transferred to a similarly sized rectangle 62a in destination bitmap 62 at

the memory addresses given in the figure. Each byte in data block 61 must be fetched (i.e., read) from a source address and written to a destination address. For example, the first byte of the data block has a source address of 19. This byte is to be transferred to a destination address of 905. The next byte for transfer has a source address of 20 and a destination address of 906, and so forth.

2. Claim 2,

Patrick illustrated, "writing pixel data to a first memory location includes writing pixel data to a first virtual memory location." in Fig. 1, number 40, which is secondary storage area that can be apply as a virtual memory. (Virtual memory is: extension of the computer's internal memory, it considers locally or remotely).

3. Claim 3,

Patrick illustrated, "The method of claim 2 further including writing pixel data to a virtual memory location associated with a memory controller client that receives pixel data written to certain virtual addresses." in Fig. 1, number 40, which is secondary storage area that can be apply as a virtual memory. (Virtual memory is: extension of the computer's internal memory, it considers locally or remotely).

4. Claim 4,

Patrick demonstrated "causing an operating system to set aside virtual addresses for said memory controller client." And the step is inherent, because the operating system provides this

options to the users to have more memory location as needed it, and these extended memory can be called virtual memory.

5. Claim 5,

Patrick demonstrated "entering an address for a second memory location includes transforming the addresses of said pixel data at said first memory location to addresses at said second memory location." And the step is inherent, because there must be an address to be able to locate pixel or any other data when transferring pixel data to second memory location.

6. Claim 6,

Patrick demonstrated "determining the offset to each pixel data by subtracting a base address at said first memory location from the address of each pixel data." And the step is inherent, because each memory location has an address tagged to the pixel data, therefore, the pixel data can be referred to previous location as if the application (recording, viewing, storing) requires. The memory location will have more space by subtracting a base address from pixel data, but the pixel data can be viewed once and it depends on the application (player, display once) requirements.

7. Claim 7,

Patrick demonstrated "adding said offset to a base address of said second memory location." And the step is inherent, because the second memory location must have the base address of current location and plus previous parameters from first memory location (here is offset).

8. Claim 8,

Patrick demonstrated "writing said transformed pixel data from said first memory location to said second memory location includes transferring said pixel data to a memory controller using a memory controller client." And the step is inherent, because Patrick shows in Fig. 1 the memory system number 30 that controls relocating the pixel data in memory areas.

9. Claim 9,

Patrick demonstrated "writing said transformed pixel data from said first memory location to said second memory location includes writing said pixel data from a first memory location associated with a first transfer function to a second memory location associated with a second transfer function." And the step is inherent, because, Patrick shows in Figs. 5 and 7 that flow charts of a method for compiling run-time code for a data block transfer.

10. Claim 10,

Patrick demonstrated "The method of claim 9 including transforming the addresses of said pixel data from addresses in a first virtual memory range associated with said first transfer function to memory addresses in a second virtual memory range associated with said second transfer function." And the step is inherent, because, Patrick shows in Figs. 5 and 7 that flow charts of a method for compiling run-time code for a data block transfer.

11. Claim 11,

Patrick discloses "write pixel data to a first memory location" in (Col. 6, lines 15-35) the following example that provides, what is involved in the block transfer of bytes from a source to a destination in memory. Patrick discloses "perform a first pixel transformation at said first memory location" in Fig. 3 is a diagram showing an 8(1, 16, 32) bit per pixel bitmap at a source (a "source bitmap or first memory location") for transfer to an 8 bpp bitmap at a destination (a "destination bitmap or second memory location"). The source bitmap 60 is located at memory addresses 0-499 (decimal) and the destination bitmap 62 is located at memory addresses 900-1399. Patrick discloses "generate a memory address for a second memory location and write said transformed pixel data from said first memory location to said second memory location" A data block 61 for transfer is contained within a rectangle 60a in source bitmap 60 and consists of 15 bytes on each of 5 consecutive scan lines at the memory addresses given in the figure. Data block 61 is to be transferred to a similarly sized rectangle 62a in destination bitmap 62 at the memory addresses given in the figure. Each byte in data block 61 must be fetched (i.e., read) from a source address and written to a destination address. For example, the first byte of the data block has a source address of 19. This byte is to be transferred to a destination address of 905. The next byte for transfer has a source address of 20 and a destination address of 906, and so forth.

12. Claim 12,

Patrick illustrated "storing instructions that enable the processor-based system to write pixel data to a first virtual memory location." in Fig. 1, number 40, which is secondary storage area

that can be apply as a virtual memory. (Virtual memory is: extension of the computer's internal memory, it considers locally or remotely).

13. Claim 13,

Patrick illustrated "storing instructions that enable the processor-based system to write pixel data to a virtual memory location associated with a memory controller client that receives pixel data written to certain virtual addresses." in Fig. 1, number 40, which is secondary storage area that can be apply as a virtual memory. (Virtual memory is: extension of the computer's internal memory, it considers locally or remotely).

14. Claim 14,

Patrick demonstrated "storing instructions that enable the processor-based system to cause an operating system to set aside virtual addresses 4 for said memory controller client." And the step is inherent, because the operating system provides this options to the users to have more memory location as needed it, and these extended memory can be called virtual memory.

15. Claim 15,

Patrick demonstrated "storing instructions that enable the processor-based system to transform the addresses of pixel data at said first memory location to addresses at said second memory location." And the step is inherent, because there must be an address to be able to locate pixel or any other data when transferring pixel data to second memory location.

16. Claim 16,

Patrick demonstrated "storing instructions that enable the processor-based system to determine the offset to each pixel data by subtracting a base address at said first memory location from the address of each pixel data." And the step is inherent, because each memory location has an address tagged to the pixel data, therefore, the pixel data can be referred to previous location as if the application (recording, viewing, storing) requires. The memory location will have more space by subtracting a base address from pixel data, but the pixel data can be viewed once and it depends on the application (player, display once) requirements.

17. Claim 17,

Patrick demonstrated "storing instructions that enable the processor-based system to add said offset to a base address of said second memory location." And the step is inherent, because the second memory location must have the base address of current location and plus previous parameters from first memory location (here is offset).

18. Claim 18,

Patrick demonstrated "storing instructions that enable the processor-based system to transfer said pixel data to a memory controller using a memory controller client." And the step is inherent, because Patrick shows in Fig. 1 the memory system number 30 that controls relocating the pixel data in memory areas.

19. Claim 19,

Patrick demonstrated "storing instructions that enable the processor-based system to write said pixel data from a first memory location associated with a first transfer function to a second memory location associated with a second transfer function." And the step is inherent, because, Patrick shows in Figs. 5 and 7 that flow charts of a method for compiling run-time code for a data block transfer.

20. Claim 20,

Patrick demonstrated "storing instructions that enable the processor-based system to transform the addresses of said pixel data from addresses in a first virtual memory range associated with said first transfer function to memory addresses in a second virtual memory range associated with said second transfer function." And the step is inherent, because, Patrick shows in Figs. 5 and 7 that flow charts of a method for compiling run-time code for a data block transfer.

21. Claim 21,

Patrick demonstrated "A system comprising: a memory controller that receives pixel data and addresses; a first memory controller client that forwards pixel data and addresses to a first transfer function; and a second memory controller client that receives data from said first transfer function together with new addresses." in (Col. 6, lines 15-35) the following example that provides, what is involved in the block transfer of bytes from a source to a destination in memory. Fig. 3 is a diagram showing an 8(1, 16, 32) bit per pixel bitmap at a source (a "source bitmap or first memory location") for transfer to an 8 bpp bitmap at a destination (a "destination bitmap or second memory location"). The source bitmap 60 is located at memory addresses 0-

499 (decimal) and the destination bitmap 62 is located at memory addresses 900-1399. A data block 61 for transfer is contained within a rectangle 60a in source bitmap 60 and consists of 15 bytes on each of 5 consecutive scan lines at the memory addresses given in the figure. Data block 61 is to be transferred to a similarly sized rectangle 62a in destination bitmap 62 at the memory addresses given in the figure. Each byte in data block 61 must be fetched (i.e., read) from a source address and written to a destination address. For example, the first byte of the data block has a source address of 19. This byte is to be transferred to a destination address of 905. The next byte for transfer has a source address of 20 and a destination address of 906, and so forth.

22. Claim 22,

Patrick demonstrated "first controller client selectively forwards pixel data and addresses to one of a plurality of transfer functions and said second controller client receives pixel data with new addresses from a plurality of transfer functions." And the step is inherent, because, Patrick shows in Figs. 5 and 7 that flow charts of a method for compiling run-time code for a data block transfer.

23. Claim 23,

Patrick demonstrated "memory controller client writes the pixel data back to said memory controller." And the step is inherent, because this is the function of memory controller.

24. Claim 24,

Patrick demonstrated "a plurality of transfer functions, one of said transfer functions arranged to write output data to an address range of another transfer function." And the step is inherent, because, Patrick shows in Figs. 5 and 7 that flow charts of a method for compiling run-time code for a data block transfer.

25. Claim 25,

Patrick demonstrated "transfer functions are associated with virtual memory address ranges." And the step is inherent, because the range of memory address must be known in order to be able to run the transfer function for any type of memory locations.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Javid A Amini whose telephone number is 703-605-4248. The examiner can normally be reached on 8-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 703-305-4713. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-8705 for regular communications and 703-746-8705 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-0377.

Javid Amini
October 1, 2002

MICHAEL RAZAVI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600